IN THE SPECIFICATION

Please amend the abstract as follows:

ABSTRACT OF THE DISCLOSURE

~~RECEIVER~~

A receiver is operable to detect a synchronisation position for recovering data from a set of received signal samples. The receiver comprises a filter having an impulse response matched to a predetermined characteristic of the received signal and is operable to produce an output signal, which is representative of the convolution of the impulse response and the received signal samples. The receiver includes a synchronisation detector operable to detect the synchronisation position from the filter output signal, and a data detector operable to detect and recover data from the set of received signal samples from the synchronisation position provided by the synchronisation detector. ~~The synchronisation detector is operable to represent each of the received signal samples as a positive or negative constant in dependence upon the relative sign of the signal sample, and to represent the samples of the filter impulse response as a positive or negative constant in dependence upon the relative sign of the impulse response samples, and the filter is operable to convolve the impulse response with the received signal samples by logically combining the representation of the received signal samples and the impulse response to produce the output signal. The receiver is therefore provided with a facility for detecting a synchronisation position from an output of the filter matched to a characteristic of the received signal.~~

~~The output signal of the matched filter is formed by logically combining the filter impulse response and the received signal samples to form a representation of a convolution but with a substantially reduced number of computations.~~

~~[No Fig.]~~

IN THE SPECIFICATION

At page 12, please amend the paragraph beginning at line 2 and ending at line 24, with the following:

As shown in Figure 5 the coarse acquisition processor comprises a correlator 204 which is arranged to receive the set of received signal samples corresponding to the COFDM symbol via a first input ~~206~~ 280. The set of received signal samples are also received via a second input ~~208~~ 282 but delayed by a period T_u corresponding to the temporal length of the data bearing signal samples of the COFDM symbol. The correlator 204 is arranged to cross correlate the two signal samples from the received signal as previously explained with reference to the previously proposed detector in Figure 2. The correlator then feeds the result of the correlation to a first moving averaging filter 206 which integrates the output of the correlation. This is in turn fed to a second moving averaging filter 208 which integrates the output of the first moving averaging filter. The output of the second moving averaging filter 208 is then integrated on a symbol by symbol basis by an integration processor 210. The integration processor 210 serves to integrate the output signal from the second moving averaging filter 208 over successive COFDM symbols so that a combined output is produced for these successive symbols. The output of the integrator 210 is then fed to a peak detector 212. The peak detector 212 is arranged to generate a peak value of the symbol integrator. However unlike the previously proposed arrangement shown in figure 2, the length of the integration over e(n) is reduced to only $N_g/4$ to make the energy peak even more biased toward the highest echo as the fine synchronisation detector depends on accurate location of the dominant path. A peak detector 212 then determines the relative

displacement which corresponds to the peak of the integrated output signal from the integrator 210 therefore providing a coarse trigger point to the fine synchronisation detector 202.

At page 13, please amend the paragraph beginning at line 13 and ending at line 30, with the following:

The fine synchronisation detector 202 is also arranged to receive the set of received signal samples and the delayed set of received signal samples from the first and second inputs ~~206, 208~~ 280, 282. The received signal samples from the first and second inputs ~~206, 208~~ 280, 282 are fed respectively to the first and second binary converters 230, 232. The output from the binary converter is fed to a first input of an adaptive matched filter 234. A second input to the adaptive matched filter is fed with samples from the output of the binary converter 232 via a delay line 236 which serves to delay each sample by a period corresponding to the number of samples within the guard period. The output of the adaptive matched filter 234 is received at an integrator 238 forming part of a synchronisation detection processor 235. The integrator 238 serves to integrate the output of the matched filter, the integrated output being presented on first and second outputs 240, 242 to a centre clip processor 244 and a centre clip level calculator 246. As will be explained shortly, the centre clip processor and the centre clip level calculator 244, 246 are arranged to pre-process the output of the adaptive matched filter which has been integrated by the integration processor 238 to the effect of cancelling various peaks of the adaptive filter output which could otherwise give a false indication of the synchronisation point. As such the performance of the synchronisation detector is improved particularly in the presence of noise.